A 69 GHz FET OSCILLATOR*

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ABSTRACT

An FET oscillator operating at V-band frequencies is presented. It has demonstrated a maximum frequency of oscillation of 69.1 GHz and an output power of 2.5 mw at 57.3 GHz.

Introduction

Until recently GaAs FETs have been primarily limited to frequencies below 18 GHz with a few notable exceptions.[1,2,3] While 0.5 micron gate length FETs have been available for several years with a theoretical f_{max} of 80 to 100 GHz, little effort has been spent on extending them to millimeter wave frequencies. FET oscillators and amplifiers offer the potential benefits of higher efficiency, lower noise and broader bandwidth when compared to Gunn and IMPATT diodes. This paper will describe the first FET oscillator to operate at V-band frequencies (50-75 GHz).

Oscillator Configuration

The approach is illustrated in Figure 1. The FET oscillator is constructed using a conventional V-band waveguide circuit originally developed for testing diodes. The reduced-height (0.020 inch) waveguide is terminated at one end by a mechanically tunable back short, and at the other end, a tapered waveguide section is used to transition to full-height V-band waveguide. The FET is mounted in a wafer which consists of the wafer body, a bias pin and a contact pin. The FET is mounted on the end of the bias pin. The gate and source are connected to the top of the bias pin with bond wires which form part of the RF circuitry. The gate is connected with minimum inductance, and the source with a 10 mil length of 0.7 mil diameter bond wire which provides an inductance of approximately 0.2 nh. A 5 mil diameter gold ball is positioned on the drain pad for contacting the press-fit drain pin. A SEM photograph of the FET mounted to the top of the bias pin is shown in Figure 2.

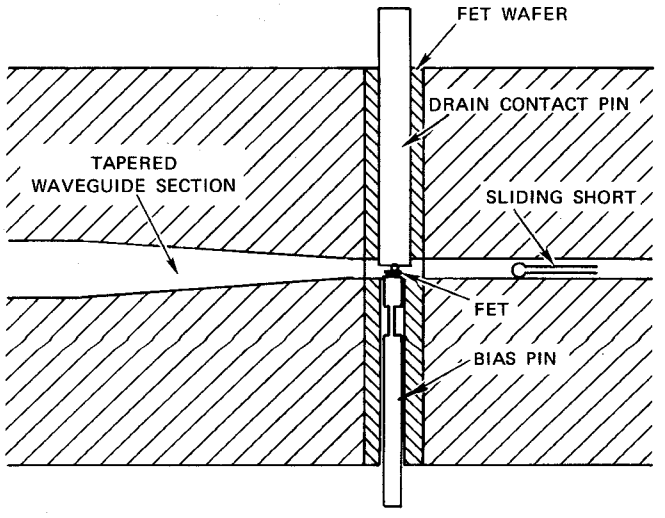

FIGURE 1: FET OSCILLATOR CIRCUIT.

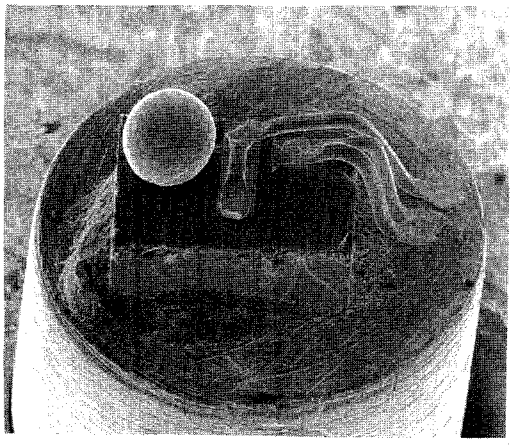

FIGURE 2: SEM OF THE FET MOUNTED ON THE END OF THE BIAS PIN.

The simplified equivalent circuit of the oscillator is shown in Figure 3. The FET with the gate and drain connected across the reduced-height waveguide forms a modified Colpitts oscillator circuit. The waveguide circuit must present a net inductive reactance to the FET at the frequency of oscillation. This is provided by the tunable back short. The source inductance (L_2) is selected such that its inductive reactance is large relative to the gate-source impedance. While its primary purpose is to supply source bias, it also prevents low frequency oscillations. This biasing scheme, which results in I_{DSS} bias, was selected for simplicity, thereby avoiding the problem of supplying a separate gate bias.

The performance of this oscillator circuit has been simulated on the computer using the device equivalent circuit model. The equivalent circuit parameters were obtained from measured S-parameters in the 2 to 18 GHz band as outlined in reference 1. The results of this simulation are shown in Figure 4 where the negative resistance of the oscillator circuit (across the waveguide) is plotted as a function of frequency. The circuit exhibits negative resistance over a broad range of frequencies extending from 24 to 70 GHz. The lower limit of the negative resistance is set by L_2 and the gate-source capacitance. By varying L_2, this lower frequency limit can be controlled over a wide range. The upper frequency limit is determined primarily by the f_T of the device and the gate propagation delay, and is approximately 70 GHz for this device. The presence of Gunn domains have not been well established, but their effect would be to add a negative conductance term in the drain circuit and raise the maximum frequency of oscillation.

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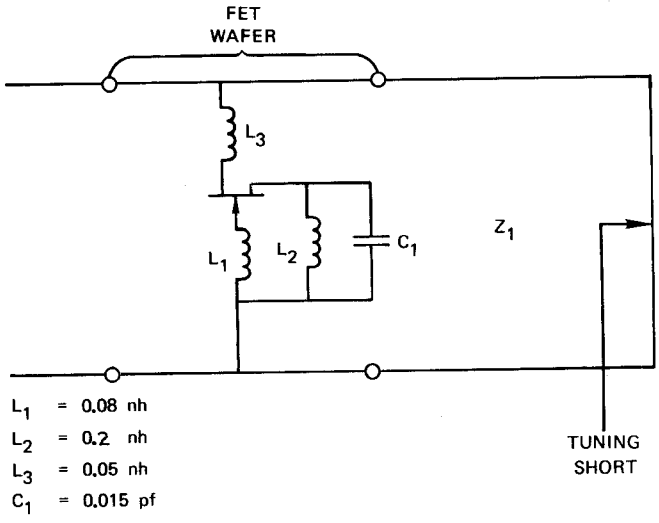

FIGURE 3: EQUIVALENT CIRCUIT OF THE FET OSCILLATOR.

Device Description

The FET used for this oscillator was an experimental device developed for Ka-band applications. All of the device patterns were generated by a direct writing E-beam system and no photolithography was used. The FET geometry, consisting of four 0.5 μm long, 75 μm wide gate fingers, is shown in Figure 5. For the oscillator, one half of the device was used by scribing at the center of the chip, and hence the total gate width was 150 μm. The channel layer was formed by a conventional vapor phase epitaxy technology with a carrier concentration of $2.4 \times 10^{17} cm^{-3}$. In order to reduce the source resistance, the deeply recessed gate was offset toward the source electrode as much as possible. The SEM picture shown in Figure 6 clearly illustrates this deeply recessed 0.5 μm long gate located immediately next to the source.

The insertion gain S_{21} of the device exhibits the unique property of relatively flat gain over the 2 to 18 GHz frequency range. The magnitude of S_{21} decreased from 7.5 dB at 2 GHz to 6 dB at 18 GHz. The extrapolated maximum frequency of oscillation, f_{max}, of this device is 75 GHz. An FET from the same lot yielded 2.3 dB noise figure with 8.1 dB associated gain at 18 GHz, and 3.7 dB noise figure with 4.0 dB gain at 29 GHz.

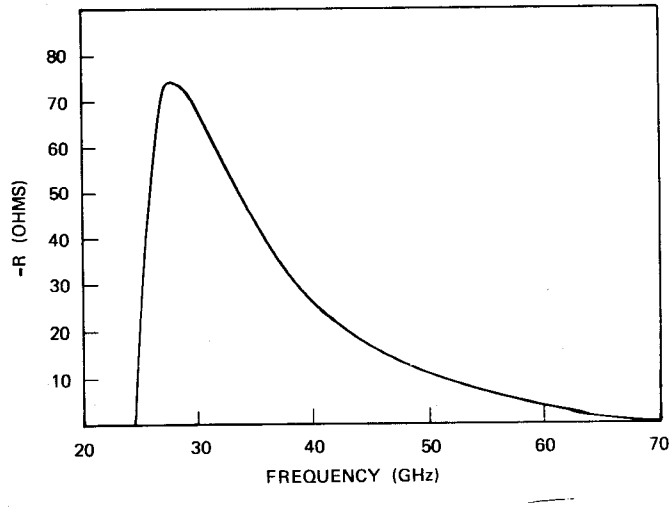

FIGURE 4: NEGATIVE RESISTANCE OF FET OSCILLATOR CIRCUIT AS A FUNCTION OF FREQUENCY.

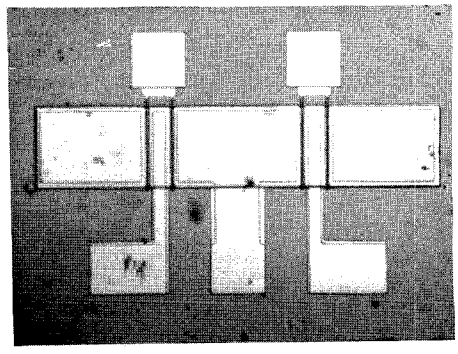

FIGURE 5: EXPERIMENTAL FET GEOMETRY.

RF Results

A prototype FET oscillator has been fabricated and tested with several different FET devices. Preliminary measurements indicate two different modes of oscillation. The first and the highest in frequency appears to be Gunn domain related. It is tunable with the back short from 66-69 GHz with an output power of typically 0.6 mw. The output power in this mode is strongly dependent upon the supply voltage and peaks at 2 volts. This fact indicates the possibility of Gunn domains contributing to oscillation. The maximum output power observed in this mode was 1 mw at 66.15 GHz with bias conditions of 2.15 volts and 37 ma.

Another lower frequency mode was observed with higher output power. As opposed to the high frequency mode, this mode demonstrated a monotonically increasing output power with supply voltage reaching 2.5 mw at 57.3 GHz with 3 volts and 41 ma. Further increases in voltage would have apparently resulted in higher power. However, the FET was destroyed mechanically before more data could be obtained. The monotonically increasing output power with supply voltage indicates that the FET is operating in the normal (non-Gunn domain) mode at this frequency.

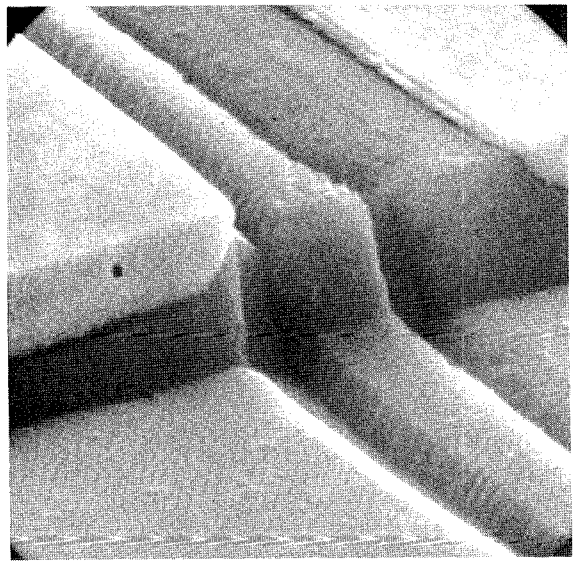

FIGURE 6: SEM OF 0.5 x 150 μm LOW NOISE FET.

Conclusion

GaAs FETs offer potential advantages over two terminal devices at millimeter wave frequencies. Among these are the easy inclusion of FETs into monolithic circuits to form the L.O. for V and W-band integrated receivers. This preliminary investigation has demonstrated the feasibility of FET oscillators at V-band and work is continuing in this exciting area.

Acknowledgement

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